

S/P 10/081818

PATENT

Applicant: Jerome M. Eldridge et al. Examiner: Tu-Tu Ho  
Serial No.: 10/081818 Group Art Unit: 2818  
Filed: February 20, 2002 Docket: 1303.045US1  
Title: ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS

#13  
I.D.S.  
G. Stenby  
8-19-04

INFORMATION DISCLOSURE STATEMENT

MS RCE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. § 1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

JEROME M. ELDRIDGE ET AL.

By their Representatives,

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Date 13 May '04

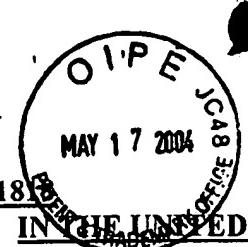
By Timothy B Clise  
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13th day of May, 2004.

Name Amy Moriarty

Signature A. Moriarty

S/N 10/081818



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS RCE  
Commissioner for Patents  
P.O. Box 1450  
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Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

| <u>Serial/Patent No.</u> | <u>Filing Date</u> | <u>Attorney Docket</u> | <u>Title</u>   |
|--------------------------|--------------------|------------------------|--|
| 09/945507                | August 30, 2001    | 1303.014US1            | FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATOR                               |
| 09/945395                | August 30, 2001    | 1303.019US1            | DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATOR |
| 09/943134                | August 30, 2001    | 1303.020US1            | PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS           |
| 09/945498                | August 30, 2001    | 1303.024US1            | INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD  |
| 09/945512                | August 30, 2001    | 1303.027US1            | IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATOR       |

**COMMUNICATION CONCERNING RELATED APPLICATIONS**

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|           |                      |             |   |
|-----------|----------------------|-------------|---|
| 09/94554  | August 30,<br>2001   | 1303.028US1 | SRAM CELLS WITH REPRESSED<br>FLOATING GATE MEMORY, LOW<br>TUNNEL BARRIER INTERPOLY<br>INSULATORS      |
| 09/945500 | August 30,<br>2001   | 1303.029US1 | PROGRAMMABLE MEMORY<br>ADDRESS AND DECODE CIRCUITS<br>WITH LOW TUNNEL BARRIER<br>INTERPOLY INSULATORS |
| 10/028001 | December<br>20, 2001 | 1303.035US1 | PROGRAMMABLE ARRAY LOGIC OR<br>MEMORY WITH P-CHANNEL<br>DEVICES AND ASYMMETRICAL<br>TUNNEL BARRIERS   |
| 10/177096 | June 21,<br>2002     | 1303.063US1 | GRADED COMPOSITION METAL<br>OXIDE TUNNEL BARRIER<br>INTERPOLY INSULATORS                              |
| 10/789038 | February<br>27, 2004 | 1303.024US2 | INTEGRATED CIRCUIT MEMORY<br>DEVICE AND METHOD  |
| 10/783695 | February<br>20, 2004 | 1303.019US2 | DRAM CELLS WITH REPRESSED<br>FLOATING GATE MEMORY, LOW<br>TUNNEL BARRIER INTERPOLY<br>INSULATORS      |
| 10/781035 | February<br>18, 2004 | 1303.063US2 | GRADED COMPOSITION METAL<br>OXIDE TUNNEL BARRIER<br>INTERPOLY INSULATORS                              |
| 10/788810 | February<br>27, 2004 | 1303.027US2 | IN SERVICE PROGRAMMABLE<br>LOGIC ARRAYS WITH LOW TUNNEL<br>BARRIER INTERPOLY INSULATORS               |
| 10/819550 | April 7,<br>2004     | 1303.019US3 | DRAM CELLS WITH REPRESSED<br>FLOATING GATE MEMORY, LOW<br>TUNNEL BARRIER INTERPOLY<br>INSULATORS      |

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Respectfully submitted,

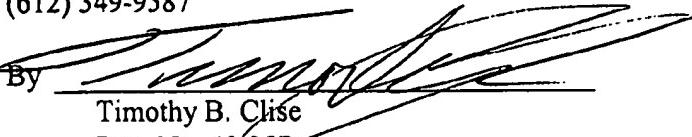
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Name

Amy Moriarty

Signature

